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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/604,819

08/19/2003

CHENG-YUAN HSU

11040-US-PA

1818

31561

7590

11/12/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE

7 FLOOR-1, NO. 100

ROOSEVELT ROAD, SECTION 2

TAIPEI, 100

TAIWAN

EXAMINER

HUYNH, ANDY

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/604,819

Applicant(s)

HSU ET AL.

Examiner

Andy Huynh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 07 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,4,6 and 7 is/are rejected.
- 7) ☒ Claim(s) 2 and 5 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

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## **DETAILED ACTION**

### ***Election/Restrictions***

In the Response to the Restriction Requirement dated November 07, 2004, Applicant has elected Group I, claims 1-7, drawn to a device and claims 8-30 are canceled without waiver, prejudice or disclaimer is acknowledged. Accordingly, claims 1-7 remain pending in this application.

### ***Priority***

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in TAIWAN on 05/22/2003. It is noted, however, that applicant has not filed a certified copy of the 92113810 application as required by 35 U.S.C. 119(b).

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 4 and 7 are rejected under 35 U.S.C. 102(e) as being anticipated by Ding (US Pub. No.: 2004/0185615A1).

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Regarding claim 4, Ding discloses in Figs. 2 and 29A and the corresponding texts as set forth in [0032]-[0095], a flash memory cell array, comprises:

- a substrate (120);

- a plurality of flash memory cell structures formed on said substrate, wherein each of said flash memory cell structures including a stack gate structure formed on said substrate and including a select gate dielectric layer (130), a select gate (140), and a gate cap layer (810), wherein said select gate dielectric layer is formed between said substrate and said select gate, and said gate cap layer is formed on said select gate;

- a spacer (2910) formed along a sidewall of said select gate;

- a control gate (170) formed on the one side of said stack gate structure and connected to said stack gate structure;

- a floating gate (160) formed between said control gate and said substrate;

- an inter-gate dielectric layer (1510) formed between said control gate and said floating gate, wherein said control gate and said floating gate constitute a stack structure;

- a tunneling dielectric layer (150) formed between said floating gate and said substrate;

and

- a drain region (BL, 174) and a source region (SL, 178) formed in said substrate, said drain region and said source region formed on the one side and the other side of said control gate and said stack gate structure respectively;

wherein said stack gate structure juxtaposes alternatively with said stack structure in said flash memory cell structures.

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Regarding claim 7, Ding discloses the flash memory cell wherein said inter-gate dielectric layer comprises silicon dioxide/silicon nitride/silicon dioxide as set forth in [0058].

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims **1, 3 and 6** are rejected under 35 U.S.C. 103(a) as being unpatentable over Ding (US Pub. No.: 2004/0185615A1) in view of Tseng (USP: 5,677,216).

Regarding claims **1 and 6**, Ding discloses in Figs. 2 and 29A and the corresponding texts as set forth in [0032]-[0095], a flash memory cell, comprises:

a substrate (120);

a stack gate structure formed on said substrate, said stack gate structure including a select gate dielectric layer (130), a select gate (140), and a gate cap layer (810), said select gate dielectric layer being formed between said substrate and said select gate, said gate cap layer being formed on said select gate;

a spacer (2910) formed along a sidewall of said select gate;

a control gate (170) formed on one side of said stack gate structure and connected to said stack gate structure;

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a floating gate (160) formed between said control gate and said substrate [and including a recess] ;

an inter-gate dielectric layer (1510) formed between said control gate and said floating gate;

a tunneling dielectric layer (150) formed between said floating gate and said substrate; and

a drain region (BL, 174) and a source region (SL, 178) formed in said substrate, wherein said drain region and said source region formed on the one side and the other side of said control gate and said stack gate structure respectively.

Ding fails to teach a floating gate including a recess and the recess is substantially filled with the control gate.

Tseng teaches in Fig. 6 that a floating gate (14) having a recess/trench filled with a control gate (22) is utilized so as to increase the surface area of the inter-poly. Therefore, a floating gate having high gate coupling ratio is achieved as set forth in the Abstract.

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form a floating gate including a recess/trench filled with a control gate, as taught by Tseng, in order to increase the surface area of the inter-poly and to have high gate coupling ratio.

Regarding claim 3, Ding discloses the flash memory cell wherein said inter-gate dielectric layer comprises silicon dioxide/silicon nitride/silicon dioxide as set forth in [0058].

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***Allowable Subject Matter***

Claims **2 and 5** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, since the prior made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Ding and Tseng, taken alone or in combination, fail to teach the claimed limitation the flash memory cell wherein a top surface of said floating gate layer is positioned between a top surface of said spacer and a top surface of said cap layer.

***Conclusion***

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Andy Huynh

Patent Examiner

Ah

10/09/04